REMARKS

The Applicant is filing a continuation pursuant to 37 C.F.R. § 1.53(b) to continue the prosecution of the parent case of this Application. In the parent case, a Final Office Action was issued on June 4, 2003. In response to that Final Office Action, the Applicant filed an Amendment pursuant to 37 C.F.R. § 1.116 to place the allowed claims and claims that were objected to in condition for allowance. In this continuation, the Applicant is canceling claims 3-9, 14-18, 20 and 21 because those claims were allowed in the parent case. Accordingly, claims 3-9, 14-18, 20 and 21 are not discussed further herein. Claims 1 and 11 are currently amended and new claims 22-24 have been added. Thus, claims 1, 2, 10-13, 19 and 22-24 are pending in the Application.

In the Final Office Action, claims 1, 2, 11-13, 23 and 24 were rejected under 35 U.S.C. § 103(a) as being obvious based on U.S. Patent No. 6,317,820 to Lopez-Aguado et al. ("the Lopez-Aguado reference") in view of U.S. Patent No. 6,317,820 to Shiell ("the Shiell reference"). Additionally, claims 10 and 19 were rejected under 35 U.S.C. § 103(a) as being obvious based on Lopez-Aguado in view of Shiell and further in view of Handy, The Cache Memory Book, ("the Handy reference"). Each of these rejections is addressed in detail below.

The Rejections Under 35 U.S.C. § 103

As set forth above, claims 1, 2, 11-13, 23 and 24 were rejected as obvious under Section 103 based on Lopez-Aguado in view of Shiell. Claims 10 and 19 were rejected under Section 103 based on Lopez-Aguado in view of Shiell and further in view of Handy. With respect to claims 1, 2, 11-13, 23 and 24, the Examiner stated:

> Claims 1-2, 11-13 and 23-24 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lopez-Aguado et al. (USPN: 6,317,810) in view of Shiell (USPN: 6,317,820). Regarding claims 1 and 23, Lopez-Aguado discloses a processor having a normal mode (normal mode occurs during cache hits) and a speculative prefetching mode (speculative mode occurs during prefetch cache hits when the prefetch bit is not asserted and when data cache misses occur, the processor operable in the speculative prefetching mode after a data cache miss comprising a first data cache for storing data when the processor operates in the normal mode (Figure 3, Reference 105; C6, L57-60) - inherently data is stored in cache 105 when a cache write hit occurs); and a second data cache for storing data in response to a store instruction only when the processor operates in the speculative prefetching mode (Figure 3, Reference 106; C6, L27-54; C6, L60-67; C7, L1-67); a first program counter for use when the processor operates in the normal mode (C4, L10-11; C5, L57-61; Figure 7, Reference 300). Lopez-Aguado does not explicitly disclose a second program counter for use only when the processor operates in the speculative prefetching mode, wherein the first program counter is configured to remain unchanged during the operation of the processor in the speculative prefetching mode. However, Shiell teaches the concept of providing a first program counter for use when a processor operates in a first mode and a second program counter for use when a processor operates in a second mode wherein the first counter is configured to remain unchanged during the operation of the processor in the second mode (C2, L24-36). This feature taught by Shiell provides efficient control logic by separating the operation of the program counters for each mode of operation, which intrinsically simplifies the control logic for controlling the program counter operations for the system. Hence, it would have been obvious to one of ordinary skill in the art to use the teachings of Shiell with the system taught by Lopez-Aguado for the desirable purpose of efficiency.
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> Regarding claim 2, Lopez-Aguado and Shiell disclose the second data cache containing an entry for storing data

(Lopez-Aguado - Figure 5), Reference DATA); and a trash bit associated with the entry, wherein the trash bit indicates whether the entry contains arbitrary (invalid) data (Lopez-Aguado - Figure 5, Reference INV).

Regarding claims 11-12 and 24, Lopez-Aguado discloses a processor having a normal mode and a speculative prefetching mode, wherein the processor operates in the speculative prefetching mode after a data cache miss occurs comprising a first register/first cache (a cache is random access memory comprised of registers, the first register consists of one of the registers in cache 105 in Figure 3) for storing data during the normal mode (normal mode occurs during data cache hits to Reference 105 of Figure 3; inherently data is stored in cache 105 when a cache write hit occurs); a second register/second data cache (the second register consists of one of the registers in cache 106 in Figure 3) for storing data only during the speculative prefetching mode (C6, L27-54; C6, L60-7; C7, L1-67); speculative prefetching mode occurs during prefetch cache hits when the PREFETCH bit is un-asserted [C6, L60-67; C7, L1-67] and after data cache misses [C6, L27-54] and data is stored in the second register only during the speculative prefetching mode), the second register comprising a first trash bit that indicates whether the second register contains arbitrary data (Figure 5, Reference INV); an instruction bus for receiving a stream of instructions including a first instruction and a second instruction (Figure 4, Reference 128; C4, L22-28); control logic for executing the first instruction (C6 , L10-13) - primary pipeline for executing the first instruction having an un-asserted LP bit); control logic for initiating a cache fill request provided execution of the first instruction encounters a data cache miss (C6, L34-48); control logic for setting the trash bit of the second register in response to the first instruction and the data cache miss (C6, L34-54); control logic for executing the second instruction in the speculative prefetching mode using the second register in place of the first register (C4, L22-34; C5, L57-67; C6, L1-4, L18-23 - when a data request (instruction) corresponding to an asserted LP bit is paired with a data request (instruction) corresponding to an un-asserted LP bit, a first request having an un-asserted LP bit is executed via the primary pipeline and accesses the data cache while the second request having an asserted LP bit is executed via the secondary pipeline and accessing the prefetch cache in place of the data cache); a first program counter for use when the processor operates in the normal mode (C4, L10-11; C5 , L57-61; Figure 7, Reference 300). Lopez-Aguado does not explicitly disclose a second program counter for use only when the processor operates in the speculative prefetching mode, wherein the first program counter is configured to remain

unchanged during the operation of the processor in the speculative prefetching mode. However, Shiell teaches the concept of providing a first program counter for use when a processor operates in a first mode and a second program counter for use when a processor operates in a second mode wherein the first counter is configured to remain unchanged during the operation of the processor in the second mode (C2, L 24-36). This feature taught by Shiell provides efficient control logic by separating the operation of the program counters for each mode of operation, which intrinsically simplifies the control logic for controlling the program counter operations for the system. Hence, it would have been obvious to one of ordinary skill in the art to use the teachings of Shiell with the system taught by Lopez-Aguado for the desirable purpose of efficiency.

Regarding claim 13, Lopez-Aguado and Shiell disclose the second data cache containing an entry for storing data (Lopez-Aguado - Figure 5, Reference DATA); and a trash bit associated with the entry, wherein the trash bit indicates whether the entry contains arbitrary (invalid) data (Lopez-Aguado - Figure 5, Reference INV).

Office Action, pages 2-5.

With respect to claims 10 and 19, the Examiner stated:

4. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lopez-Aguado (USPN: 6,317,810) in view of Shiell (USPN: 6,317,820) as applied to claims 1 and 11 above and further in view of Handy, The Cache Memory Book.

Lopez-Aguado and Shiell disclose the second data cache as an associative cache (Lopez-Aguado - C4, L46-50), however, Lopez-Aguado does not disclose the first cache as a direct mapped cache. Handy teaches that direct mapped caches are the simplest most common way to design a cache (Lopez-Aguado - Page 54, Paragraph 1, last two lines). Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement Lopez-Aguado's first cache as a direct mapped cache for the desirable purpose of simplification.

Office Action, pages 5-6.

The Applicant respectfully traverses these rejections. The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).

Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

In the present case, the combination of Lopez-Aguado and Shiell cannot render the Applicant's claims obvious under Section 103 because that combination does not include all of the elements recited in the Applicant's claims. Specifically, independent claim 1 requires "a first program counter for use when the processor operates in the normal mode" and "a second program counter for use only when the processor operates in the speculative prefetching mode, *wherein the first program counter is configured to remain unchanged during operation of the processor in the speculative prefetching mode.*" (Emphasis added.) Independent claims 11 and 24 contain analogous limitations.

The Examiner correctly concedes that Lopez-Aguado does not disclose a processor that includes a second program counter that is used when the processor operates in a speculative prefetching mode. The Examiner asserts that the missing elements are found in the Shiell reference. In fact, the teachings of the Shiell reference are not at all applicable to the Applicant's claimed invention or the Lopez-Aguado reference. Moreover, Shiell does not teach, suggest or illustrate the second program counter required by the Applicant's claims. The program counters disclosed in Shiell are completely different.

Shiell discloses a processor that is capable of operating in a first mode in which only a single instruction is processed during each instruction cycle or a second superscalar mode in which multiple instructions are processed in each instruction cycle. *See* Shiell, Abstract. Contrary to the Examiner's assertions, however, the program counters described in Shiell are used in both operational modes:

> This invention is a very long instruction word data processor including plural data registers, plural functional units and plural program counters. The data processor may be selectively operable in either a first or second mode. *In the first mode program instructions are executed by selected ones of the data*

> *registers and selected ones of the functional units, under the control of a predetermined program counter. In the second mode a first program counter controls execution of program instructions using a first group of data registers and a first group of functional units, and a second program counter controls execution of program instructions using a disjoint second group of data registers and a disjoint second group of functional units.*
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> Shiell, column 2, lines 24-36 (Emphasis added).

The only reason for the existence of the second program counter in the Shiell device is to operate in conjunction with the first program counter when the processor is operating in superscalar mode. In other words, Shiell teaches that multiple program counters may be used to support multiple parallel operational units. This is not the Applicant's invention. Shiell does not teach the use of multiple program counters in support of *alternative* operational modes as required by the Applicant's independent claims requiring a first program counter that supports a normal operational mode and a second program counter that supports a speculative prefetching mode. The second program counter is used *instead of* the first program counter when the processor switches from the normal operational mode into the speculative prefetching mode. Thus, Shiell does not disclose a program counter as recited in the Applicant's independent claims. Accordingly, the combination of Lopez-Aguado and Shiell cannot render the Applicant's claims obvious because that combination does not disclose every element of those claims.

In addition, the combination of Lopez-Aguado and Shiell is not proper because the Examiner has failed to meet the required burden of articulating a motivation for the modification of the device disclosed in Lopez-Aguado with elements taken from Shiell. The Examiner concedes that Lopez-Aguado fails to disclose "a second program counter for use only when the processor operates in the speculative prefetching mode, wherein the first

program counter is configured to remain unchanged during the operation of the processor in the speculative prefetching mode." Because Lopez-Aguado does not disclose the use of a second program counter for a speculative prefetching mode, it is not possible for Lopez-Aguado to contain any suggestion or teaching of the desirability of that structure.

The Examiner relies on Shiell only for the teaching of generally employing a second program counter. Thus, the Examiner tacitly concedes that Shiell is missing any disclosure that teaches, suggests or illustrates the use of a second program counter *in connection with a processor that employs a speculative prefetching mode*. Because neither Lopez-Aguado nor Shiell teaches the use of a second program counter that operates in a prefetching mode and not in normal mode, there can be no teaching, suggestion or illustration (outside of the Applicant's own disclosure) in support of the Examiner's Section 103 rejections based on Lopez-Aguado in combination with Shiell.

As for the motivation of one of ordinary skill in the art to employ the teachings of Shiell in combination with the teachings of Lopez-Aguado, the Examiner states:

> Lopez-Aguado does not explicitly disclose a second program counter for use only when the processor operates in the speculative prefetching mode, wherein the first program counter is configured to remain unchanged during the operation of the processor in the speculative prefetching mode. However, Shiell teaches the concept of providing a first program counter for use when a processor operates in a first mode and a second program counter for use when a processor operates in a second mode wherein the first counter is configured to remain unchanged during the operation of the processor in the second mode (C2, L 24-36). *This feature taught by Shiell provides efficient control logic by separating the operation of the program counters for each mode of operation, which intrinsically simplifies the control logic for controlling the program counter operations for the system. Hence, it would have been obvious to one of ordinary skill in the art to use the*

teachings of Shiell with the system taught by Lopez-Aguado for the desirable purpose of efficiency.

Office Action, pages 4-5 (Emphasis added).

The Examiner's statements are nothing more than assertions about the teachings of Lopez-Aguado and Shiell, not a convincing line of reasoning *why* one of skill in the art would add combine those teachings. Under the Examiner's standard of obviousness, any two references in a generally related field of endeavor could be combined for the "desirable purpose of efficiency" regardless of whether the teachings of the references had any relationship to each other at all. This is not the law.

In a similar situation, the Federal Circuit recently overturned the Board, which had upheld an examiner's rejection. In *In re Lee*, 61 U.S.P.Q.2d 1430 (Fed. Cir. 2002), the examiner rejected the applicant's claims under 35 U.S.C. § 103 without giving an appropriate supporting motivation to combine references. The Board subsequently affirmed the examiner's rejection. In overturning the Board's decision, the Federal Circuit stated that:

> When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness. *See, e.g., McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 U.S.P.Q.2d 1001, 1008 (Fed. Cir. 2001) ("the central question is whether there is reason to combine [the] references, "a question of fact drawing on the Graham factors).
>
> 'The factual inquiry whether to combine references must be through and searching.' *Id.* It must be based on objective evidence of record. This precedent has been reinforced in myriad decisions, and cannot be dispensed with. [citations omitted].

Lee, 61 U.S.P.Q.2d at 1433.

In the present case, the Examiner's assertions about why one of ordinary skill in the art would be motivated to combine the teachings of Lopez-Aguado with the teachings of Shiell does not meet the evidentiary standard required for obviousness under Section 103. The reasoning cited by the Examiner is not "thorough and searching" and it does not address "the central question [of] whether there is reason to combine [the] references." Indeed, the Examiner's assertions represent nothing more than the use of impermissible hindsight in conjunction with the teachings of the Applicant's own disclosure. There can be no *prima facie* case of obviousness based on the combination of Lopez-Aguado and Shiell. This is true because elements of the Applicant's independent claims 1, 11 and 24 are clearly missing from Lopez-Aguado, and the Examiner has provided no legally supportable basis for adding those elements from Shiell, even if Shiell contained the correct elements.

For at least these reasons, the combination of Lopez-Aguado and Shiell fails to meet the limitations of independent claims 1, 11 and 24. Accordingly, the Applicant respectfully requests that the rejection of claims 1, 11 and 24, and the claims dependent thereon not be repeated.

As set forth above, claims 10 and 19 were rejected under Section 103 based on Lopez-Aguado in view of Shiell and further in view of Handy. The Applicant respectfully asserts that the rejection of claims 10 and 19 is defective for at least the reasons set forth above with respect to independent claims 1, 11 and 24. The Handy reference is relied on by the Examiner only to show a direct-mapped cache in contrast to an associative cache. Handy is not asserted by the Examiner to provide the teaching of a second program counter that is admittedly missing from Lopez-Aguado and demonstrably missing from Shiell. Accordingly,

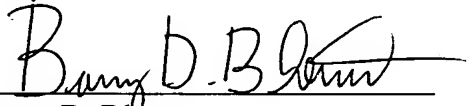
the Applicant respectfully asserts that no combination of Lopez-Aguado, Shiell and Handy can render the Applicant's amended claims obvious. The Applicant respectfully requests that the rejection of claims 10 and 19 under Section 103 based on Lopez-Aguado in view of Shiell and further in view of Handy not be repeated.

Conclusion

In view of the amendments and remarks set forth above, the Applicant respectfully requests that the Examiner not repeat the rejections made during prosecution of the parent case to this Application. Furthermore, the Applicant asserts that an indication of the allowability of claims 1, 2, 10-13, 19 and 22-24 is appropriate. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: October 24, 2003



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